

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/602,089
 Priority Filing Date June 22, 2000
 Inventor Kevin L. Beaman et al.
 Assignee Micron Technology, Inc.
 Priority Group Art Unit 2818
 Priority Examiner David Nhu
 Attorney's Docket No. MI22-2475
 Title: Semiconductor Assemblies, Methods of Forming Structures over Semiconductor
 Substrates, and Methods of Forming Transistors Associated with Semiconductor
 Substrates

INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/602,089, filed June 22, 2000, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). As a courtesy, Applicant submits copies of the cited foreign references and articles for review.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 1-13-04


 D. Brent Kenady
 Reg. No. 40,045

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2475		SERIAL NO.	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Kevin L. Beaman et al.			
				FILING DATE		GROUP Unknown	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,032,545	07/91	Doan et al.			
	AB	5,436,481	07/95	Egawa et al.			
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	AK	5,719,083	06/95	Komatsu			
	AL	5,760,475	11/94	Cronin			
FOREIGN PATENT DOCUMENTS							
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							Yes No
	AM	WO 96/39713	12/96	PCT			
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		Wolf, S., "Silicon Processing for the VLSI Era", Lattice Press 1990, Vol. 2, pp. 212-213.				
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	AT		Ko, L. et al., "The Effect of Nitrogen Incorporation into the Gate Oxide by Using Shallow Implantation of Nitrogen and Drive-In Process", IEEE 1996, pp. 32-35.				
EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

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	AA	5,834,372	12/95	Lee			
	AB	5,619,057	04/96	Komatsu			
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	AD	6,054,396	04/00	Doan			
	AE	6,174,821	01/01	Doan			
	AF	5,939,750	08/99	Early			
	AG	5,254,489	10/93	Nakata			
	AH	5,464,792	11/95	Tseng et al.			
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	AL	6,093,661	07/00	Trivedi et al.			
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	AR		Doyle, B. et al., "Simultaneous Growth of Different Thickness Gate Oxides in Silicon CMOS Processing", IEEE Vol. 16 (7), July 1995,				
			pp. 301-302.				
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			Technology Digest of Technical Papers, IEEE 1994, pp. 107-108.				
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	AB	5,674,788	10/97	Wristers et al.			
	AC	5,596,218	01/97	Soleimani et al.			
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	AG	6,114,203	09/00	Ghidini et al.			
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	AI	6,091,110	07/00	Herbert et al.			
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	AK	6,140,187	10/00	DeBusk et al.			
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	AA	6,399,445 B1	06/02	Hattangady et al.			
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